Sub Code: R2021042 **R20** **Set No. 1**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY-GURUJADA VIZIANAGARAM
II B. Tech I Semester Supplementary Examinations, November – 2024
SWITCHING THEORY AND LOGIC DESIGN
(ECE)

Time: 3 hours **Max. Marks: 70**

Answer any FIVE Questions
ONE Question from Each unit
All Questions Carry Equal Marks
*****

1	a)	Convert the following i) $(1000)_2 = ( )_{gray}$ ii) $(100001001.1101)_2 = ( )_8$ iii) $(22.64)10 = ( )16$ iv) $(A72E)_{16} = ( )_8$	[7]
	b)	Perform the subtraction using 1's compliment and 2's compliment method i) $(5C)_{16}$ - $(3F)_{16}$ ii) $(C0)_{16}$ - (7A)16	[7]
		(OR)	
2	a)	Realize 2 input X-OR and X-NOR gate using minimum number of NAND gates	[7]
	b)	If the Hamming code sequence of 1100110 is transmitted, consider any one position as error at receiving end and locate the position of error if any.	[7]
3	a)	Simply F = Σ m (0, 1,3,7,10, 12) + d (14,15) and implement using minimum number of NOR gates.	[7]
	b)	Design 4 bit adder subtractor circuit	[7]
		(OR)	
4	a)	Find the reduced POS form of the function, F (A, B, C, D) = ∑ m (1, 3, 7, 9, 11, 15)	[7]
	b)	Design a BCD adder and explain its operation	[7]
5	a)	Implement f (A,B,C,D) = ∑(0,1,4,5,6,7,9,10,12,13,15) using PLA and explain its procedure.	[7]
	b)	A combinational circuit is defined by the functions F1 (A, B, C) = ∑ (3, 5, 6,7) and F2 (A, B, C) = ∑ (0, 2, 4, 7), Implement the circuit with a PLA having three inputs, four product terms, and two outputs.	[7]
		(OR)	
6	a)	Design 5 to 32 decoder using one 2 to 4 decoder and four 3 to 8 decoders.	[7]
	b)	Implement the following Boolean function using 8:1 Multiplexer F (A, B, C, D)=∑m (0,1,3,4,8,9,15)	[7]
7	a)	Convert SR Flip Flop to T Flip Flop and JK Flip Flop to SR Flip Flop	[7]
	b)	Explain the race around condition in J-K flip-flop and give a method to eliminate it.	[7]

(OR)

8	a)	What is shift register? Explain with the help of block diagram 4-bit register with parallel load.	[7]
	b)	Demonstrate the operation 4-stage ring counter using D-flip flops.	[7]
9	a)	Design a sequence detector which detects sequence '1010' for Mealy machine in overlapping.	[7]
	b)	Design a sequence detector which detects sequence '1101' for Moore machine in overlapping.	[7]

(OR)

10	a)	What are the difference between Mealy and Moore Machine	[7]
	b)	Discuss about finite state machine, state diagram, and state table.	[7]

*****